

## Overvoltage Protection for 2-Series to 5-Series Cell Li-Ion Batteries with Internal Delay Timer

Check for Samples: [bq771800](#), [bq771801](#), [bq771802](#), [bq771803](#)

### FEATURES

- 2-, 3-, 4-, and 5-Series Cell Overvoltage Protection
- Internal Delay Timer
- Fixed OVP Threshold
- High-Accuracy Overvoltage Protection:  $\pm 10$  mV
- Low Power Consumption  $I_{CC} \approx 1 \mu\text{A}$  ( $V_{CELL(ALL)} < V_{PROTECT}$ )
- Low Leakage Current Per Cell Input  $< 100$  nA

- Small Package Footprint
  - 8-pin QFN (3 mm × 4 mm)

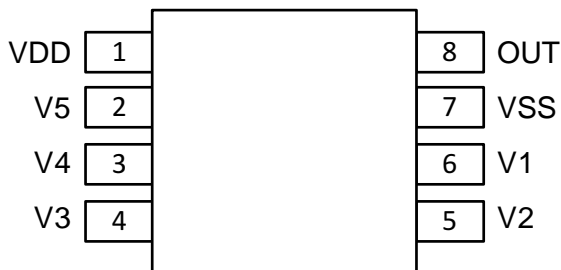
### APPLICATIONS

- Protection in Li-Ion Battery Packs in:
  - Power Tools
  - UPS Battery Backup
  - Light Electric Vehicles (eBike, eScooter, Pedal Assist Bicycles)

### DESCRIPTION

The bq7718xy family of products is an overvoltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition.

In the bq7718xy device, an internal delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output is triggered into its active state (either high or low depending on the configuration). For quicker production-line testing, the bq7718xy device provides a Customer Test Mode with greatly reduced delay time.



**Figure 1. bq771800 Pinout**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION

T <sub>A</sub>	Part Number	Package	Package Designator	OVP (V)	OV Hysteresis (V)	Output Delay	Output Drive	Tape and Reel (Large)	Tape and Reel (Small)
-40°C to 110°C	bq771800	8-Pin QFN	DPJ	4.300	0.300	4 s	CMOS Active High	bq771800DPJR	bq771800DPJT
	bq771801			4.275	0.050	3 s	NCH Active Low, Open Drain	bq771801DPJR	bq771801DPJT
	bq771802			4.225	0.300	1 s	NCH Active Low, Open Drain	bq771802DPJR	bq771802DPJT
	bq771803			4.275	0.050	1 s	NCH Active Low, Open Drain	bq771803DPJR	bq771803DPJT
	bq7718xy <sup>(1)</sup>			3.850–4.650	0–0.300	1 s	NCH, Active Low, Open Drain	bq7718xyDPJR	bq7718xyDPJT

(1) Future option, contact TI.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		bq7718xy	UNITS
		8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	56.6	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	56.4	
$\theta_{JB}$	Junction-to-board thermal resistance	30.6	
$\Psi_{JT}$	Junction-to-top characterization parameter	1.0	
$\Psi_{JB}$	Junction-to-board characterization parameter	37.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	11.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

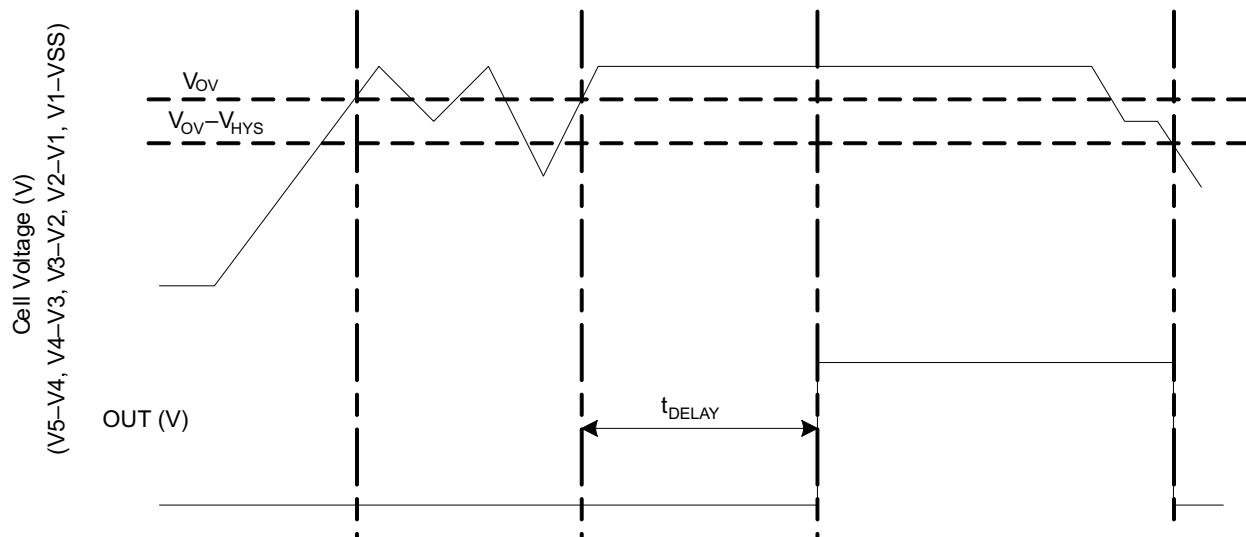
## PIN FUNCTIONS

bq7718xy	Pin Name	Type I/O	Description
1	VDD	P	Power supply
2	V5	I	Sense input for positive voltage of the fifth cell from the bottom of the stack
3	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
4	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
5	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
6	V1	I	Sense input for positive voltage of the lowest cell in the stack
7	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
8	OUT	O	Output drive for overvoltage fault signal

## PIN DETAILS

In the bq7718xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference,  $V_{OV}$ . If any cell voltage exceeds the programmed OV value, a timer circuit is activated. When the timer expires, the OUT terminal goes from inactive to active state.

For NCH Open Drain Active Low configurations, the OUT pin pulls down to VSS when active (OV present) and is high impedance when inactive (no OV).



**Figure 2. Timing for Overvoltage Sensing**

### Sense Positive Input for $V_x$

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

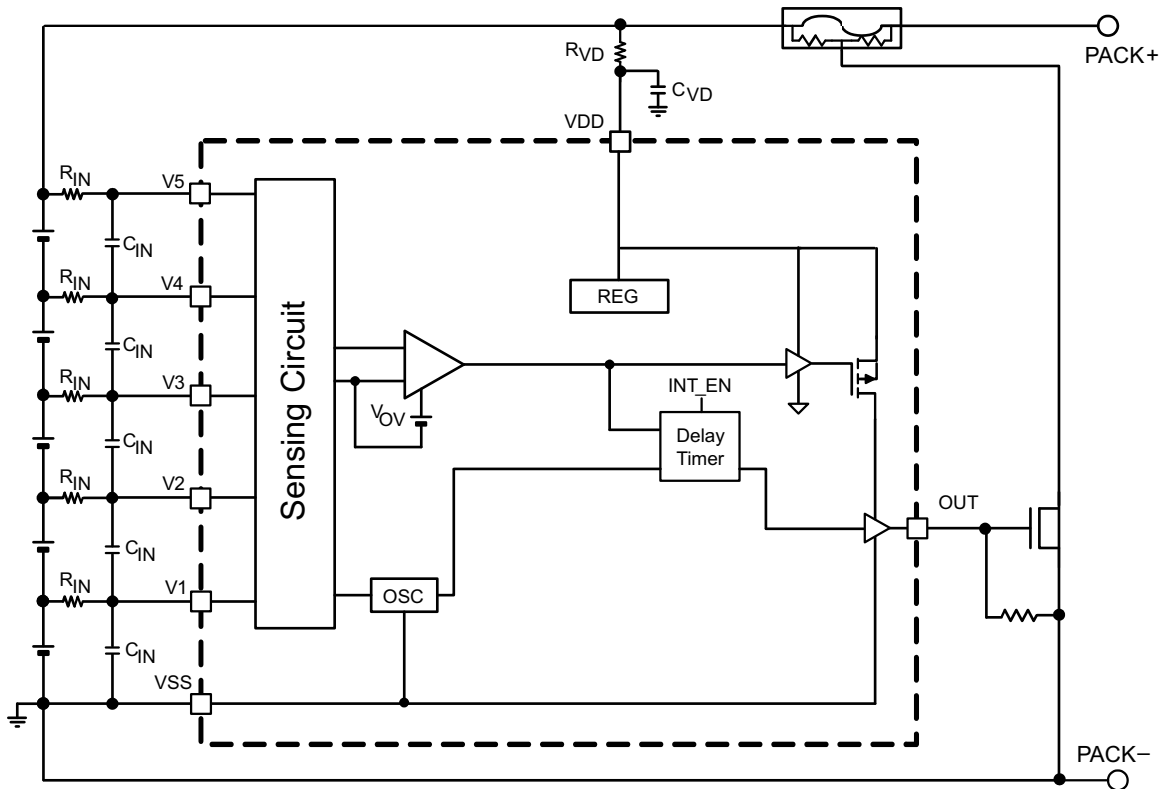
### Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either active HIGH or LOW options.

### Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	CONDITION	VALUE/UNIT
Supply voltage range	VDD–VSS	–0.3 to 30 V
Input voltage range	V5–VSS or V4–VSS or V3–VSS or V2–VSS or V1–VSS	–0.3 to 30 V
Output voltage range	OUT–VSS	–0.3 to 30 V
Continuous total power dissipation, P <sub>TOT</sub>		See package dissipation rating.
Functional temperature		–40 to 110°C
Storage temperature range, T <sub>STG</sub>		–65 to 150°C
Lead temperature (soldering, 10 s), T <sub>SOLDER</sub>		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>DD</sub> <sup>(1)</sup>	3		25	V
Input voltage range	0		5	V
	V5–V4 or V4–V3 or V3–V2 or V2–V1 or V1–VSS			
Operating ambient temperature range, T <sub>A</sub>	–40		110	°C

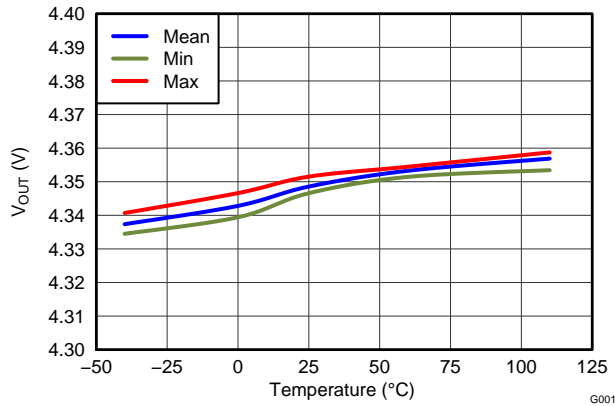
(1) See [APPLICATION SCHEMATIC](#).

## DC CHARACTERISTICS

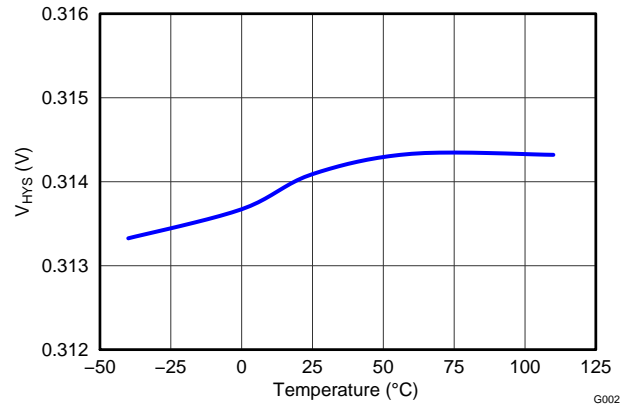
Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 18\text{ V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $110^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$  to  $25\text{ V}$  (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
<b>Voltage Protection Threshold VCx</b>						
$V_{OV}$	$V_{(PROTECT)}$ Overvoltage Detection	bq771800		4.300		V
		bq771801, bq771803		4.275		V
		bq771802		4.225		V
$V_{HYS}$	OV Detection Hysteresis	bq771800	250	300	400	mV
		bq771801, bq771803	0	50	100	V
		bq771802	250	300	400	mV
$V_{OA}$	OV Detection Accuracy	$T_A = 25^\circ\text{C}$	-10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	$T_A = -40^\circ\text{C}$	-40		44	mV
		$T_A = 0^\circ\text{C}$	-20		20	mV
		$T_A = 60^\circ\text{C}$	-24		24	mV
		$T_A = 110^\circ\text{C}$	-54		54	mV
<b>Supply and Leakage Current</b>						
$I_{CC}$	Supply Current	$(V_5-V_4) = (V_4-V_3) = (V_3-V_2) = (V_2-V_1) = (V_1-V_{SS}) = 4.0\text{ V}$ (See <a href="#">Figure 13.</a> )		1	2	$\mu\text{A}$
$I_{IN}$	Input Current at $V_x$ Pins	$(V_5-V_4) = (V_4-V_3) = (V_3-V_2) = (V_2-V_1) = (V_1-V_{SS}) = 4.0\text{ V}$ (See <a href="#">Figure 13.</a> )	-0.1		0.1	$\mu\text{A}$
<b>Output Drive OUT, CMOS Active HIGH Versions Only</b>						
$V_{OUT1}$	Output Drive Voltage, Active High	$(V_5-V_4), (V_4-V_3), (V_3-V_2), (V_2-V_1),$ or $(V_1-V_{SS}) > V_{OV}, V_{DD} = 18\text{ V}, I_{OH} = 100\ \mu\text{A}$	6			V
		If three of four cells are short circuited and only one cell remains powered and $> V_{OV}, V_{DD} = V_x$ (cell voltage), $I_{OH} = 100\ \mu\text{A}$		$V_{DD} - 0.3$		V
		$(V_5-V_4), (V_4-V_3), (V_3-V_2), (V_2-V_1),$ and $(V_1-V_{SS}) < V_{OV}, V_{DD} = 18\text{ V}, I_{OL} = 100\ \mu\text{A}$ measured into pin		250	400	
$I_{OUTH1}$	OUT Source Current (during OV)	$(V_5-V_4), (V_4-V_3), (V_3-V_2), (V_2-V_1),$ or $(V_1-V_{SS}) > V_{OV}, V_{DD} = 18\text{ V}, \text{OUT} = 0\text{ V}.$ Measured out of OUT pin			4.5	mA
$I_{OUTL1}$	OUT Sink Current (no OV)	$(V_5-V_4), (V_4-V_3), (V_3-V_2), (V_2-V_1),$ and $(V_1-V_{SS}) < V_{OV}, V_{DD} = 18\text{ V}, \text{OUT} = V_{DD}.$ Measured into OUT pin	0.5		14	mA
<b>Output Drive OUT, NCH Open Drain Active LOW Versions Only</b>						
$V_{OUT2}$	Output Drive Voltage, Active Low	$(V_5-V_4), (V_4-V_3), (V_3-V_2), (V_2-V_1),$ or $(V_1-V_{SS}) > V_{OV}, V_{DD} = 18\text{ V}, I_{OL} = 100\ \mu\text{A}$ measured into OUT pin		250	400	mV
$I_{OUTH2}$	OUT Sink Current (during OV)	$(V_5-V_4), (V_4-V_3), (V_3-V_2), (V_2-V_1),$ or $(V_1-V_{SS}) > V_{OV}, V_{DD} = 18\text{ V}, \text{OUT} = V_{DD}.$ Measured into OUT pin	0.5		14	mA
$I_{OUTL2}$	OUT Source Current (no OV)	$(V_5-V_4), (V_4-V_3), (V_3-V_2), (V_2-V_1),$ and $(V_1-V_{SS}) < V_{OV}, V_{DD} = 18\text{ V}, \text{OUT} = V_{DD}.$ Measured out of OUT pin			100	nA
<b>Delay Timer</b>						
$t_{DELAY}$	OV Delay Time	bq771800	3.2	4	4.8	s
		bq771801	2.4	3	3.6	s
		bq771802, bq771803	0.8	1	1.2	s
		Preview option only. Contact TI.	4.4	5.5	6.6	s
$X_{CTMDELAY}$	Fault Detection Delay Time during Customer Test Mode	See .		15		ms

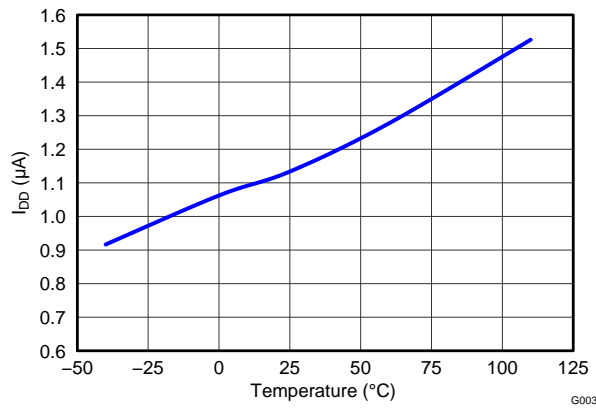
## TYPICAL CHARACTERISTICS



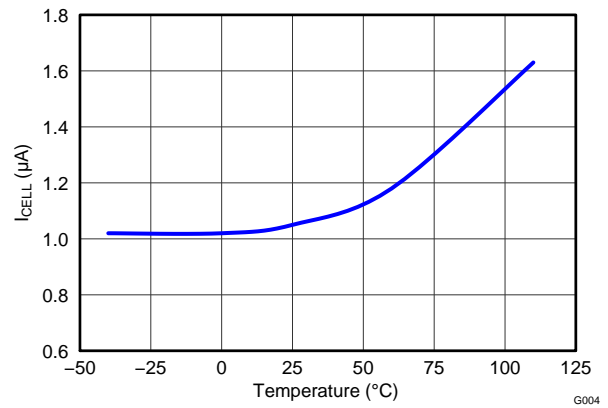
**Figure 3. Overtolerance Threshold (OVT) vs. Temperature**



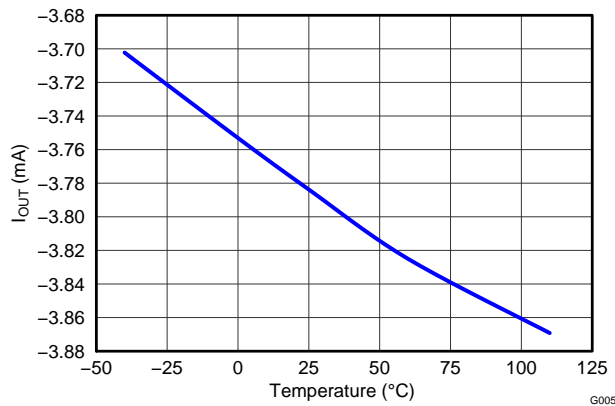
**Figure 4. Hysteresis  $V_{HYS}$  vs. Temperature**



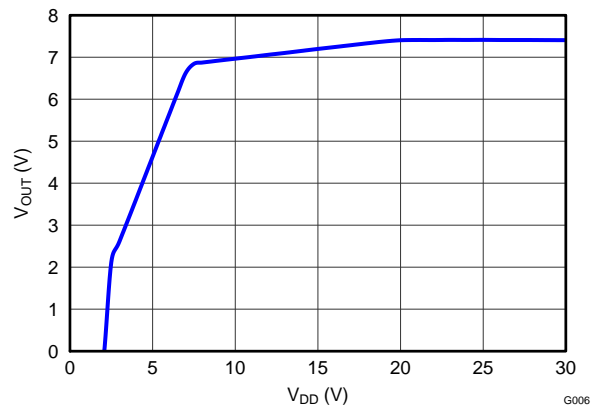
**Figure 5.  $I_{DD}$  Current Consumption vs. Temperature at  $V_{DD} = 16\text{ V}$**



**Figure 6.  $I_{CELL}$  vs. Temperature at  $V_{CELL} = 9.2\text{ V}$**



**Figure 7. Output Current  $I_{OUT}$  vs. Temperature**



**Figure 8.  $V_{OUT}$  vs.  $V_{DD}$**

APPLICATION INFORMATION

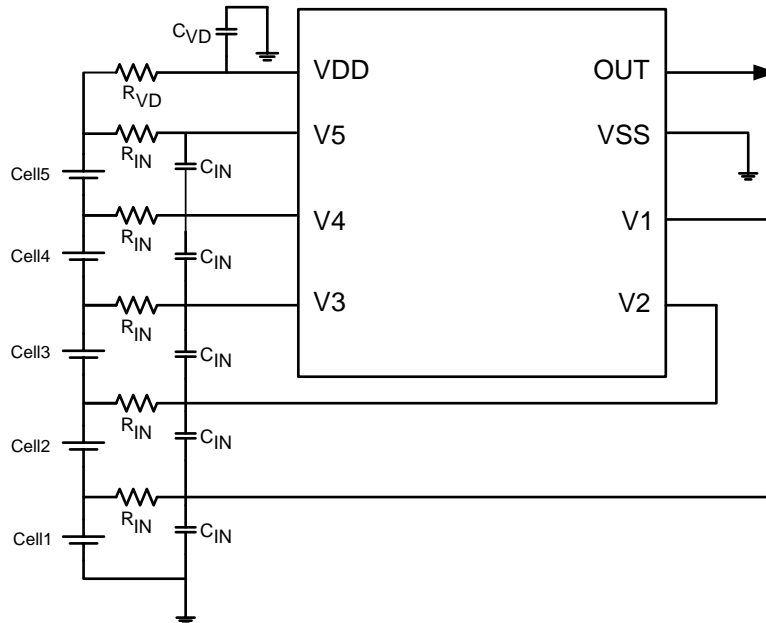


Figure 9. Application Configuration

NOTE

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements.

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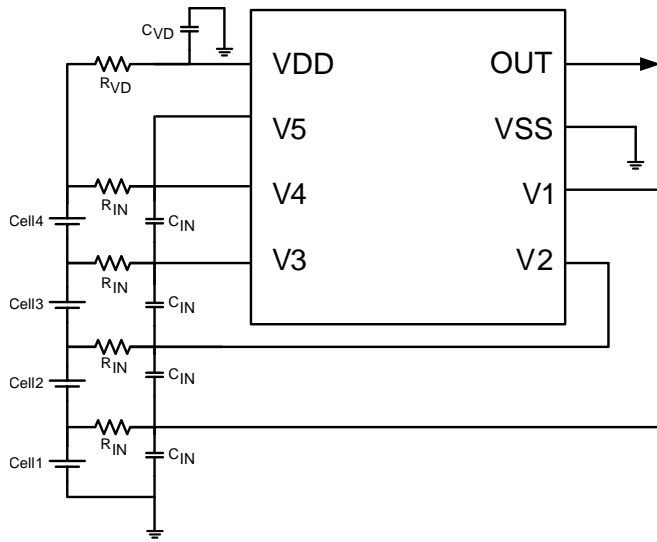
Table 1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R <sub>IN</sub>	900	1000	1100	Ω
Voltage monitor filter capacitance	C <sub>IN</sub>	0.01		0.1	μF
Supply voltage filter resistance	R <sub>VD</sub>	100		1K	Ω
Supply voltage filter capacitance	C <sub>VD</sub>		0.1		μF
CD external delay capacitance			0.1	1	μF
OUT Open drain version pull-up resistance to PACK+			100		kΩ

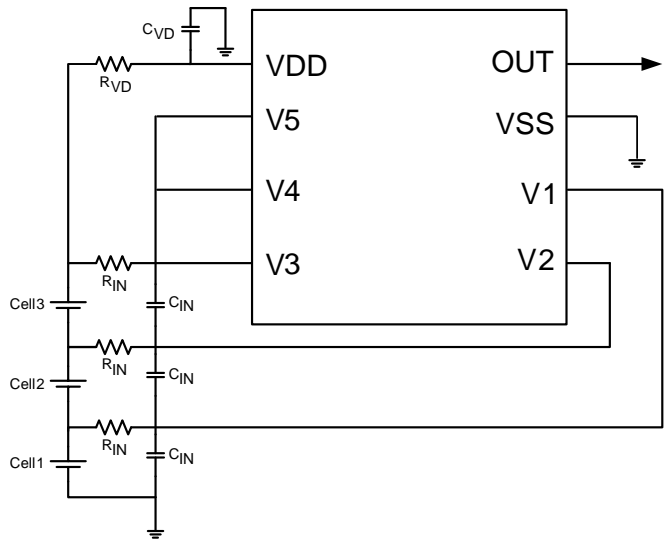
NOTE

The device is calibrated using an R<sub>IN</sub> value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V<sub>OV</sub> trigger level.

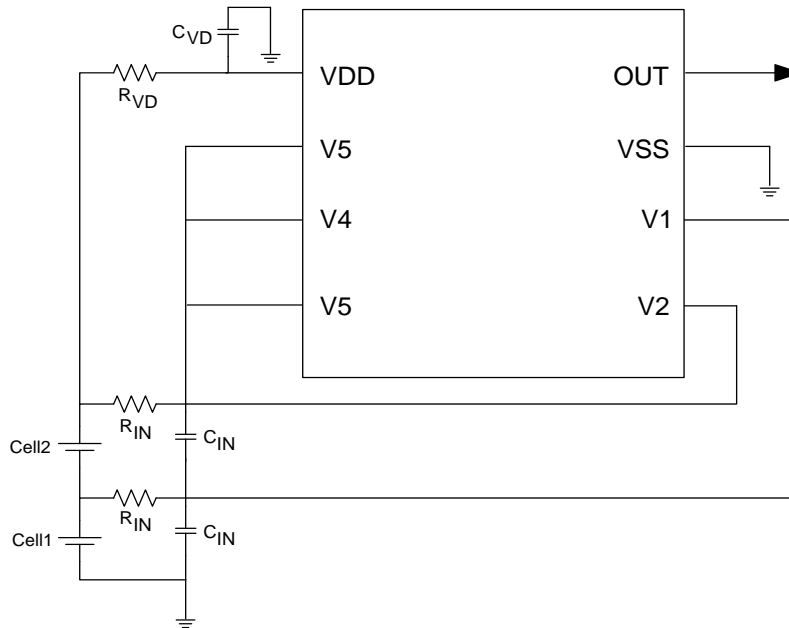
**APPLICATION SCHEMATIC**



**Figure 10. 4-Series Cell Configuration**



**Figure 11. 3-Series Cell Configuration with Fixed Delay**



**Figure 12. 2-Series Cell Configuration with Internal Fixed Delay**

**NOTE**

In these application examples, an external pull-up resistor is required on the OUT terminal to configure for an Open Drain Active Low operation.

## CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V5 (see Figure 13). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to V5 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

### CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V5–V4), (V4–V3), (V4–V3), (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 13 shows the timing for the Customer Test Mode.

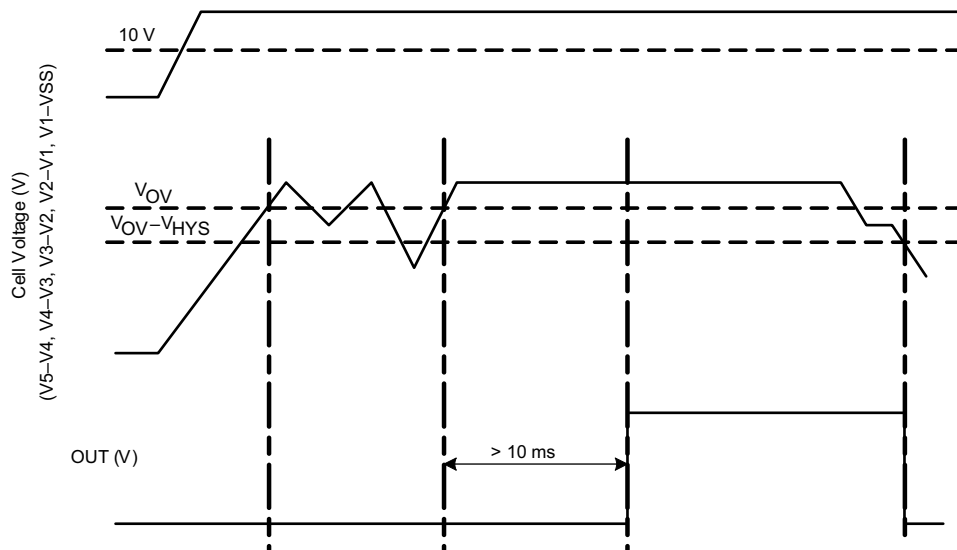


Figure 13. Timing for Customer Test Mode

Figure 14 shows the measurement for current consumption for the product for both VDD and Vx.

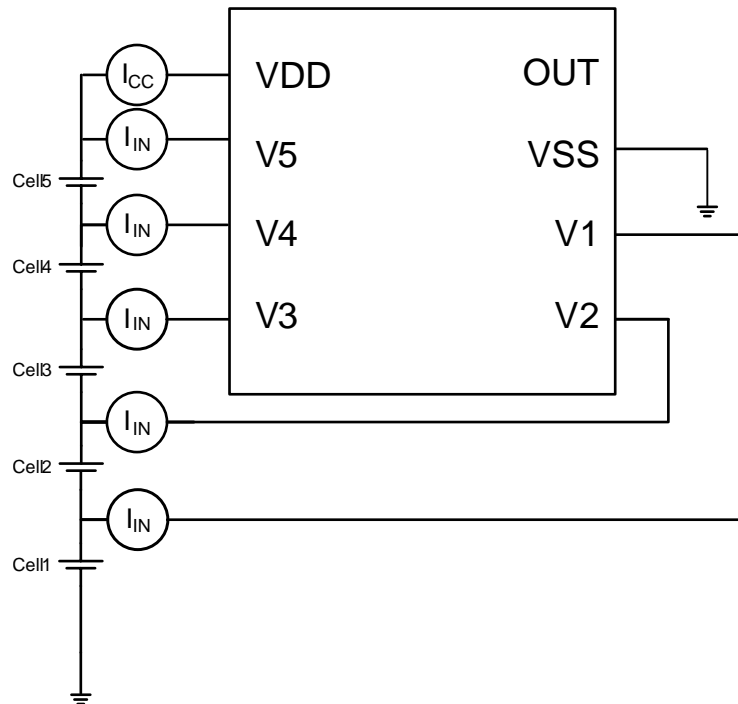
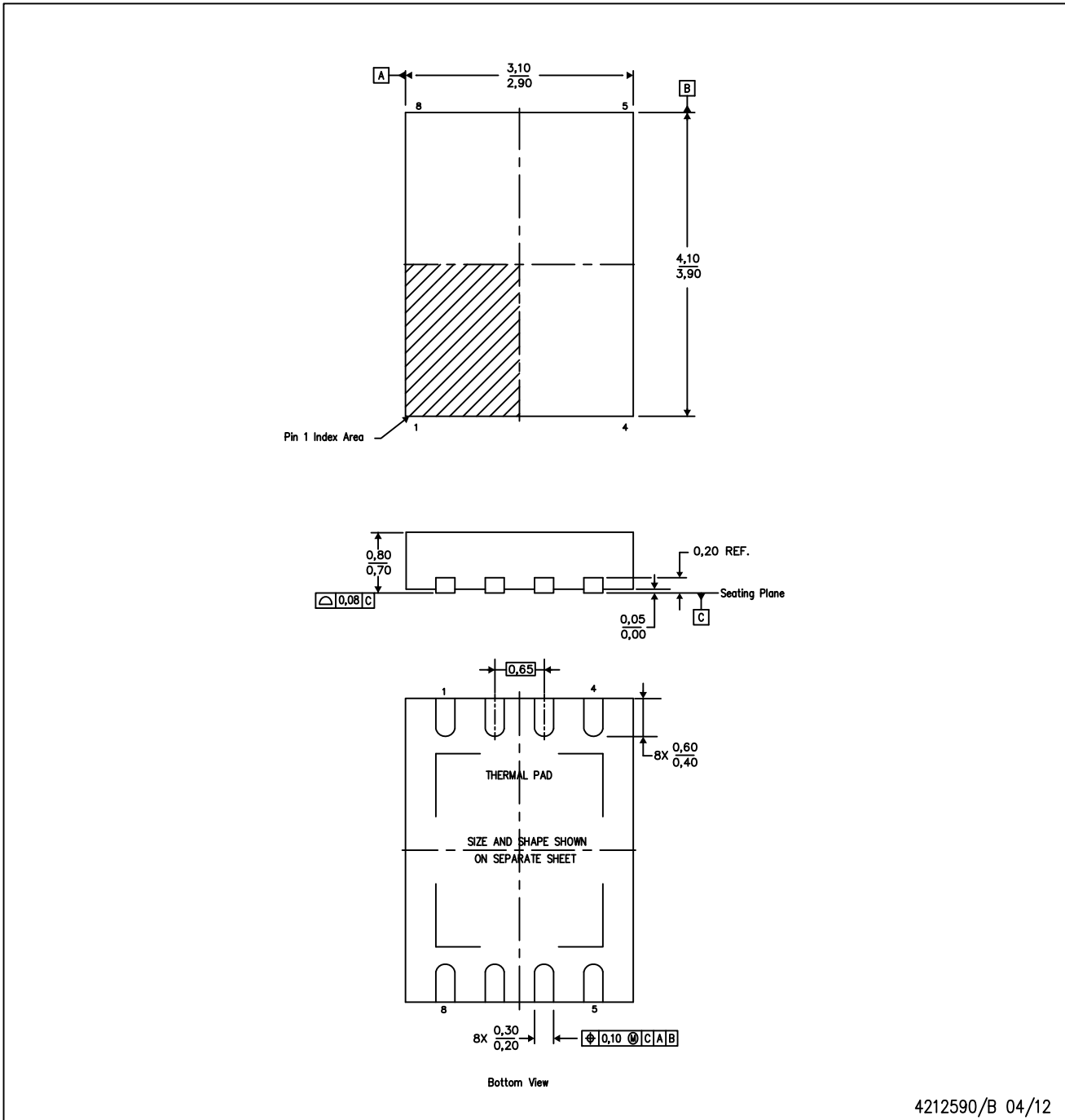


Figure 14. Configuration for IC Current Consumption Test

DPJ (R-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4212590/B 04/12

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ771800DPJR	PREVIEW	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ771800DPJT	PREVIEW	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ771801DPJR	PREVIEW	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ771801DPJT	PREVIEW	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ771802DPJR	PREVIEW	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ771802DPJT	PREVIEW	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ771803DPJR	PREVIEW	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
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